## REMARKS

The applicant has carefully considered the Office action dated October 25, 2004, and the references it cites. In the Office action, claims 6-15 are rejected under 35 U.S.C § 103(a) as unpatentable over Ramdani et al. in view of Kub et al. The applicant respectfully traverses the rejections and believes the claims as filed to be allowable over the cited art. In view of the following, it is respectfully submitted that all pending claims are in condition for allowance and favorable reconsideration is respectfully requested.

The applicant respectfully submits that independent claim 6 is allowable over the art of record. Specifically, Ramdani et al. fail to teach or suggest forming an uppermost metal interconnect on a semiconductor substrate, or forming an oxide layer on the substrate *and* the uppermost metal interconnect. The Office action incorrectly contends that although Ramdani et al. do not teach forming an uppermost metal interconnect on a substrate, one would overcome this deficiency by looking to the disclosure of Kub et al. which describes forming an uppermost metal interconnect. However, the applicant respectfully submits that one would not be motivated to combine Ramdani et al. and Kub et al. to form an uppermost metal interconnect on a semiconductor substrate, or to form an oxide layer on the substrate *and* the uppermost metal interconnect as recited in claim 6. As set forth below, although the applicant does not concede that one would be motivated to combine Ramdani et al. and Kub et al., as explained in detail below, even if one were to combine those references, that combination would not teach or suggest the method recited in claim 6.

Ramdani et al. describes a method for fabricating a semiconductor structure including a metal oxide interface with silicon by "form[ing] a silicate seed layer *necessary for the subsequent growth* of monocrystalline alkaline-earth metal oxide layers." (col. 3, lines 12-13; emphasis added). The crux of the Ramdani et al. patent is "the [stable silicate] *novel interface* between a silicon substrate and one or more layers of a high dielectric constant

(high-k) metal oxide." (col. 3, lines 16-18; emphasis added). However, modifying Ramdani et al., as the Office action suggests, to form an uppermost metal interconnect on a semiconductor substrate as recited in claim 6 *would prevent* growing the silicate seed layer (20) Ramdani et al. identify as "necessary" to their invention, at least in the areas where the metal interconnects are formed.

More specifically, Ramdani et al. describe forming the silicate seed layer (2) using a silicon dioxide layer (14) and a metal oxide layer (18). Ramdani et al. further describe forming the silicon dioxide layer (14) on the silicon substrate (10) by exposing the silicon substrate (10) to oxygen. Ramdani et al. state that "$SiO_2$ ... is desirable for purposes of growing the seed layer material on the substrate to create the [stable silicate (20)] interfacial layer." (col. 3, lines 25-27). If one were to place a metal interconnect on the substrate of Ramdani et al., the process described in Ramdani et al. would not result in the formation of an oxide layer on the substrate *and* the uppermost metal interconnect as recited in claim 6. Ramdani et al. specifically described forming the silicon dioxide layer (14) on the silicon substrate (10) by exposing the silicon substrate (10) to oxygen. Exposing a metal interconnect to oxygen does not form a silicon dioxide layer on the metal interconnect. Thus, Ramdani et al makes no provision to form a silicon dioxide layer on a metal interconnect. In contrast, claim 6 requires "forming an oxide layer on the substrate and the uppermost metal interconnect." Thus, the proposed modification of Ramdani et al. does not meet the recitations of claim 6.

Kub et al. do not overcome the deficiencies of Ramdani et al. Although the applicant does not concede that one would be motivated to combine Ramdani et al. and Kub et al., even if one were to combine those references, Kub et al. do not teach or suggest forming an oxide layer on the substrate and the uppermost metal interconnect as recited in claim 6. Instead, Kub et al. describe depositing a silicon nitride layer (52) on the conductive paths (47,48).

(col. 4, lines 53-56). As discussed above, Ramdani et al. also fail to disclose forming an oxide layer on the uppermost metal interconnect. Thus, because neither Ramdani et al. nor Kub et al. teach or suggest forming an oxide layer on the uppermost metal interconnect, irrespective of how one combines Ramdani et al. and Kub et al., one does not arrive at the combination of claim 6.

Further, Kub et al. do not teach or suggest forming an uppermost metal interconnect on the semiconductor substrate as recited in claim 6. Kub et al. describe forming a silicon oxide layer (35) on a semiconductor substrate (33) and then forming conductive paths (47, 48) on an "upper surface 36 *of [the] silicon oxide layer 35*." (col. 4, lines 26-28; col. 4, lines 49-52). Therefore, Kub et al. do not teach forming an uppermost metal interconnect on the semiconductor substrate as recited in claim 6. The Office action conceded that Ramdani et al. do not teach or suggest forming an uppermost metal interconnect on a semiconductor substrate. Because neither Ramdani et al. nor Kub et al. teach or suggest forming an uppermost metal interconnect on the semiconductor substrate, irrespective of how one combines Ramdani et al. and Kub et al., one does not arrive at the combination of claim 6.

Furthermore, in addition to forming an uppermost metal interconnect on a semiconductor substrate and forming an oxide layer on the substrate and the uppermost metal interconnect, claim 6 requires forming an aluminum layer on the oxide layer, and forming a stress-relief layer on the aluminum layer to reduce stress on the metal interconnect. Nowhere do either Ramdani et al. or Kub et al. teach or suggest forming an oxide layer on an uppermost metal interconnect, forming an aluminum layer on the oxide layer and a stress relief layer on the aluminum layer *to reduce stress on the uppermost metal interconnect*." As discussed above, Ramdani et al. has no uppermost metal interconnect. On the other hand, the uppermost metal interconnect of Kub et al. is layer number 80 (see col. 5, line 40-44). As shown in FIG. 14 of Kub et al., there is only one layer on this uppermost interconnect 80 (i.e.,

the passivation layer 85), not an oxide layer, an aluminum layer, and a stress-relief layer as recited in claim 6.

In view of the foregoing, the applicant respectfully submits that independent claim 6 and all claims depending therefrom are in condition for allowance. If the Examiner is of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is invited to contact the undersigned at the number identified below.

Respectfully submitted,

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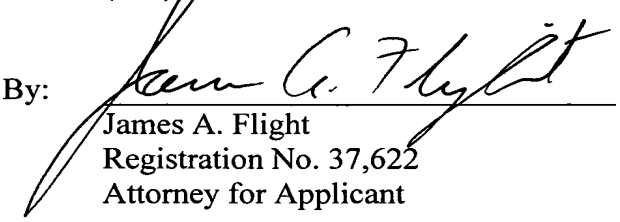
By: 

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